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| 09/838,743 | 04/19/2001 | Gerald Deboy | GR 99 P 2591 P | 9326 |

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| EXAMINER |
|---|
| MONDT, JOHANNES P |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2826 | |

DATE MAILED: 06/06/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/838,743 | DEBOY ET AL. | |
| | Examiner | Art Unit | |
| | Johannes P Mondt | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-11 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-6 and 8-11 is/are rejected.

7)☒ Claim(s) 7 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 7 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

### *Information Disclosure Statement*

The examiner has considered the items listed in the Information Disclosure Statement filed 5/15/01 as Paper No. 3

### *Specification*

The specification does not relate (nor define) the charge $q_c$ (see pages 14-15) in terms of well-defined attributes of the device, but instead simply introduces a quantity appearing in the claim language as "a critical charge quantity in the semiconductor body and is linked to an electric field applied between the first and second electrodes by Maxwell equation", without actually relating said charge $q_c$ to anything concrete, not even implicitly through Maxwell's equations (I believe the Applicant means Poisson's equation in particular). Poisson's equation relates charge density to the local surplus of electrostatic potential. Any charge should be defined in terms of an integral over a well-defined charge density distributed in space or to a charge content assumed, for simplicity, to be located in some definite point location. As a result, the present invention with regard to claim 2 suffers from lack of enablement. Appropriate re-editing of the specification is required.

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. ***Claim 2*** is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In particular, the critical charge density is not linked to an electric field applied between said first and second electrode by Maxwell's equation (Poisson's equation, that is) unless a charge distribution is provided as well. Poisson's equation merely connects the charge density to the local surplus of the electrostatic potential. This is not enough information, not for people of ordinary, - nor for those of extra-ordinary skills in the art, to determin $q_c$. Referring to Applicant's specification, on page 3, in which the relation between critical field and critical charge, here indicated by $Q_c$, is discussed: the location and distribution of charges determines the electric field distribution, not merely a number of dimension charge. Applicant would need to relate $q_c$ to actual attributes of the semiconductor material, such as the critical electric field at which the semiconductor material undergoes breakdown at physically infinitesimal volume elements, and its electrostatic environment, in order to render the inquality that forms the essence of claim 2 into an operational, well-defined imperative, without which the present claim lacks enablement.

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. ***Claim 1*** is rejected under 35 U.S.C. 102(b) as being anticipated by the conference publication by Laska et al (IEDM 90-807-810). Laska et al teach (cf. Figure 1) a vertically structured power semiconductor component, comprising:

a semiconductor body of first conductivity type (n type) and having a first main surface (upper main surface of $n^-$ region) and a second main surface opposite said first main surface (bordering the lowest region marked "p");

a body zone (the highest region marked "p") of a second conductivity type (p type), i.e., opposite of said first conductivity type, introduced into said first main surface;

a zone (marked "n") of said first conductivity type (n type) disposed in said body zone;

a first electrode E making contact with said zone and with said body zone;

a second electrode disposed on said second main surface;

an insulating layer disposed on said first main surface (the insulating layer does feature on Figure 1, however is not explicitly indicated therein as such. However, the gate, to be discussed in the sequel is identified, while the device taught by Laska et al is a IGBT type device, i.e., insulated gate bipolar transistor; and hence the presence of said insulating layer between the gate and the substrate is inherent in the device);

a gate electrode G disposed above said body zone and separated from said body zone by said insulating layer; and an intersection of said

semiconductor body and said body zone defining a pn junction (namely the common border between said semiconductor body and body zone), said semiconductor body having a layer thickness between said pn junction and said main surface selected such that when the maximum allowed blocking voltage or a voltage just less than said maximum allowed blocking voltage is applied between said first electrode and said second electrode, a space charge zone created in said semiconductor body meets said second main surface before a field strength created by an applied blocking voltage reaches a critical value (cf. page 807, second column, from line 8 down).

In conclusion, Laska et al anticipate claim 1.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. ***Claim 3*** is rejected under 35 U.S.C. 103(a) as being unpatentable over the conference publication by Laska et al (IEDM 90-807), in view of Hutchings et al (5,387,528). As detailed above, Laska et al anticipate claim 1 (on which claim 3 depends). Laska et al do not necessarily teach the further limitation defined by claim 3. However, it has long been standard in the art to dispose at the second main surface in

IGFET devices a heavily doped semiconductor terminal regions of the same conductivity type as the substrate, as evidenced by Hutchings (heavily doped semiconductor terminal regions 4a (cf. column 6, lines 14-19), so as to mitigate the large drop in conductivity between the electrode on said main second surface and the lowly doped semiconductor substrate 4. Because the purpose of Laska is to increase breakdown voltage of power IGFET devices whilst local gradients in the electrostatic potential determine whether a local breakdown condition is met, the motivation for the incorporation of the teachings in the above-described sense by Hutchings into the invention taught by Laska is evident. The inventions can be combined simply by replacement of the bottom part of the semiconductor body by a heavily doped semiconductor layer of the same type as said semiconductor body. Success in implementing the invention can thus be reasonably expected.

5. ***Claims 1 and 3-5*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Park (5,702,961) in view of the conference publication by Laska et al (IEDM 90-807-810).

*With regard to claim 1:* Park teaches (cf. Figure 1) a vertically structured power semiconductor component (cf. abstract, first sentence), comprising:

a semiconductor body of first conductivity type (n type) comprising subregions 104, 116 and 100 (cf. column 3, line 56, column 4, line 23, and column 6, line 45) and having a first main surface (upper main surface of the latter) and a second main surface opposite said first main surface (lower main surface of the latter);

a body zone 108 of a second conductivity type (p type), i.e., opposite of said first conductivity type, introduced into said first main surface (cf. column 4, lines 1-2);

a zone 110 of said first conductivity type (n type) disposed in said body zone (cf. column 4, lines 14-18);

a first electrode 114 making contact with said zone and with said body zone (cf. column 4, lines 27-28);

a second electrode 112 (cf. column 3, line 65) disposed on said second main surface;

an insulating layer disposed on said first main surface (the insulating layer does feature on Figure 1, however this is not explicitly indicated therein as such. However, the gate, to be discussed in the sequel is identified, while the device taught by Park is a IGBT type device, i.e., insulated gate bipolar transistor; and hence the presence of said insulating layer between the gate and the substrate is inherent in the device);

a gate electrode 118 (cf. column 4, line 19) disposed above said body zone and separated from said body zone by said insulating layer; and an intersection of said semiconductor body and said body zone defining a pn junction (namely the common border between said semiconductor body and body zone).

*Park does not necessarily teach* said semiconductor body to have a layer thickness between said pn junction and said main surface selected such that

when the maximum allowed blocking voltage or a voltage just less than said maximum allowed blocking voltage is applied between said first electrode and said second electrode, a space charge zone created in said semiconductor body meets said second main surface before a field strength created by an applied blocking voltage reaches a critical value. However, Laska et al, as discussed above, do teach this (cf. page 807, second column, from line 8 down) for the obvious reason to optimize thickness for improving the blocking voltage. Because blocking voltage improvement also is an objective of Park (see column 1, left column) there exists motivation to combine the references. Combination of the teachings by park and Laska et al is possible, because all that is needed is an appropriate selection for the thickness of the semiconductor body. Expectation of success in combing the references is reasonable, considering the independence of said thickness of all other limitations in claim 1.

*With regard to claim 3:* the semiconductor body taught by Park has heavily doped terminal regions 100 of first conductivity type (n-type) disposed at said second main surface.

*With regard to claim 4:* Park teaches the preferential inclusion of a further zone 116 of said first conductivity type disposed in the vicinity of said second main surface (cf. column 3, line 53).

*With regard to claim 5:* Park teaches punch-through regions disposed between said heavily doped terminal regions (cf. regions 102-100-102-100 alternating in doping

type). The statement in claim 5 on current control is inherent in the device limitation stated up to this point in the claim.

6. ***Claim 6*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Park and Laska et al (IEDM 90-807-810) as applied to claim 1 above, and further in view of Fruth et al (6,011,280), or, -in the alternative, as being unpatentable over Laska et al (IEDM 90-807-810) in view of Fruth et al (6,011,280). As detailed above, Laska et al anticipate claim 1, while claim 1 also is unpatentable over Park in view of Laska et al. Neither Laska et al nor Park necessarily teach the further limitation defined by claim 6. However, the application of (a) edge termination 34/30 and a (b) channel stop 40 to mitigate the effect of geometrically enhanced edge electric fields through screening provided by dopants and for the purpose of termination the device region, respectively, is well known in the art, as witnessed by Fruth et al (see column 1, line 56 – column 2, line 16).

7. ***Claims 8-10*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Park and Laska et al as applied to claim 1 above, and in further view of Yamaguchi et al (5,821,586); or, in the alternative as being unpatentable over Laska et al in view of Yamaguchi et al. Claim 1 was shown to be anticipated by Laska et al and to be unpatentable over Park in view of Laska et al (see above). Neither park nor Laska et al necessarily teach the further limitation defined by claim 8. However, the inclusion of a compensating region in the form of a p-conductive column underneath a more heavily and oppositely doped semiconductor region in contact with metal is well-known in the art of vertical transistors, as shown by Yamaguchi et al (cf. column 3, lines 19-31) for

the purpose of providing a trigger element compensating for excessive voltage between the first and second electrode. The teaching by Yamaguchi et al can be readily combined with those of Park and Laska et al, or, in the alternative with those of Laska et al, because only the inclusion of a an additional doping step is required to create the compensation region. Motivation stems from the higher voltage that can be achieved by inclusion of the compensating region without causing breakdown. Furthermore, success of the combination can be reasonably expected because p-doping techniques are readily available and well tested.

*With regard to claim 9:* although both epitaxy and implantation operations are used by Yamaguchi to create said compensation region (cf. column 3, lines 61-67 and column 4, line 1), the further limitation defined by claim 9 does not constitute any further device limitation upon the invention: not the method of making but instead the device itself is the subject matter of the present claim, considering the claim is about a vertically structured power semiconductor component.

*With regard to claim 10:* said compensation region of second conductivity type taught by Yamaguchi et al is produced horizontally between said main surface and said second main surface through the same implantation openings.

8. ***Claim 11*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Park and Laska et al as applied to claim 1 above, and further in view of Yamamoto (JP404234173A); or, in the alternative, over Laska et al (IEDM 90-807-810), in view of Yamamoto (JP404234173A). As detailed above, claim 1 is anticipated by Laska et al, and, also is unpatentable over Park in view of Laska et al. Neither Laska et al not Park

necessarily teach the further limitation of claim 11. However, in view of the increased values of electric fields in edge regions due to geometric effects, the inclusion of edge regions of a conductivity type opposite to that of the semiconductor body region to compensate for excessive voltage as part of voltage protection is well known in the art of vertical transistors, as witnessed by Yamamoto (cf. abstract and constitution).

### *Allowable Subject Matter*

9. ***Claim 7*** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***10.*** The following is a statement of reasons for the indication of allowable subject matter: the magneto-resistance positioned at the location indicated in the specification as part of a vertical transistor structure has not been found in the literature to date.

### *Conclusion*

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Okabe et al (5,973,338); Bhagat (4,636,830); Chow et al (4,901,127).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
May 30, 2002

NATHAN J. FLYNN
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